Description

SG1622 is a LCD controller with 32x8 memory mapping driver. It is especially designed for low power operation, extra timer function, and simple control interface and so on. These make SG1622 most suitable for the MCU application.

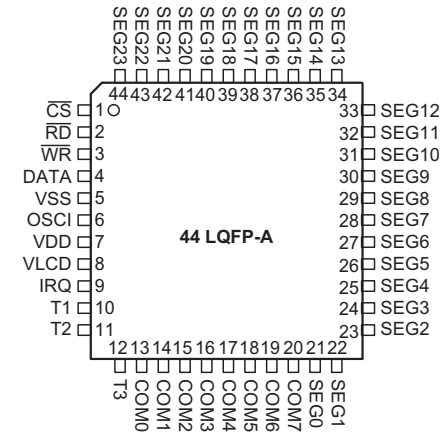
Features

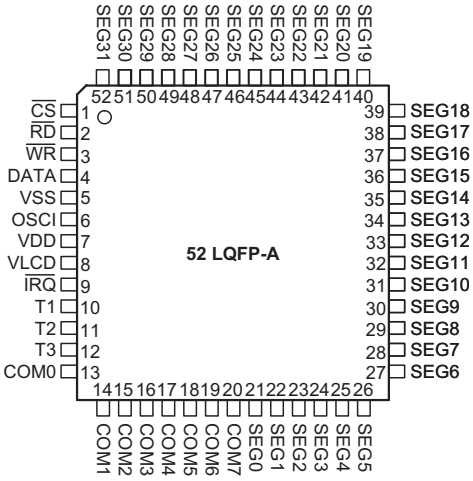
- Operating voltage: 2.7V~5.2V
- 1/4 bias, 1/8 duty, frame frequency is 64Hz
- Max. 32×8 patterns, 8 commons, 32 segments
- Built-in internal resistor type bias generator
- 3-wire serial interface
- 8 kinds of time base or WDT selection
- Time base or WDT overflow output
- Built-in LCD display RAM
- R/W address auto increment
- Two selectable buzzer frequencies (2kHz or 4kHz)
- Power down command reduces power consumption
- Software configuration feature
- Data mode and Command mode instructions
- Three data accessing modes
- VLCD pin to adjust LCD operating voltage
- Built-in RC oscillator

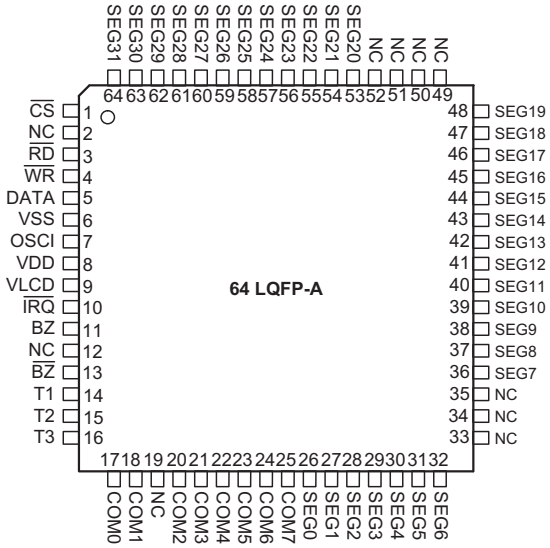
General Description

SG1622 is a peripheral device specially designed for I/O type MCU used to expand the display capability. The max. display segment of the device are 256 patterns (32×8). It also supports serial interface, buzzer sound, Watchdog Timer or time base timer functions. The SG1622 is a memory mapping and multi-function LCD controller. The software configuration feature of the SG1622 make it suitable for multiple LCD applications including LCD modules and display subsystems. Only three lines are required for the interface between the host controller and the SG1622.

Pin Assignment







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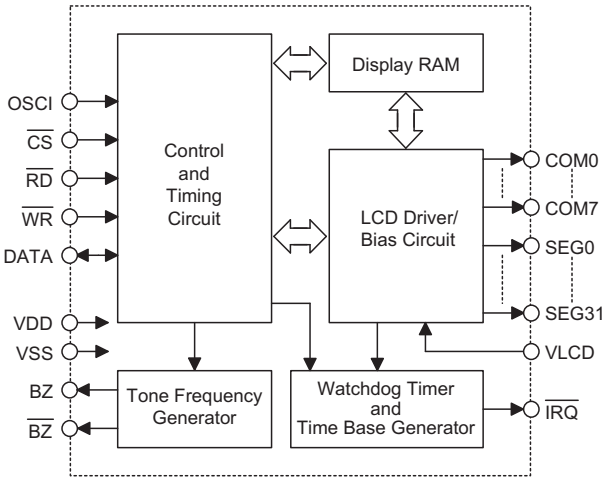
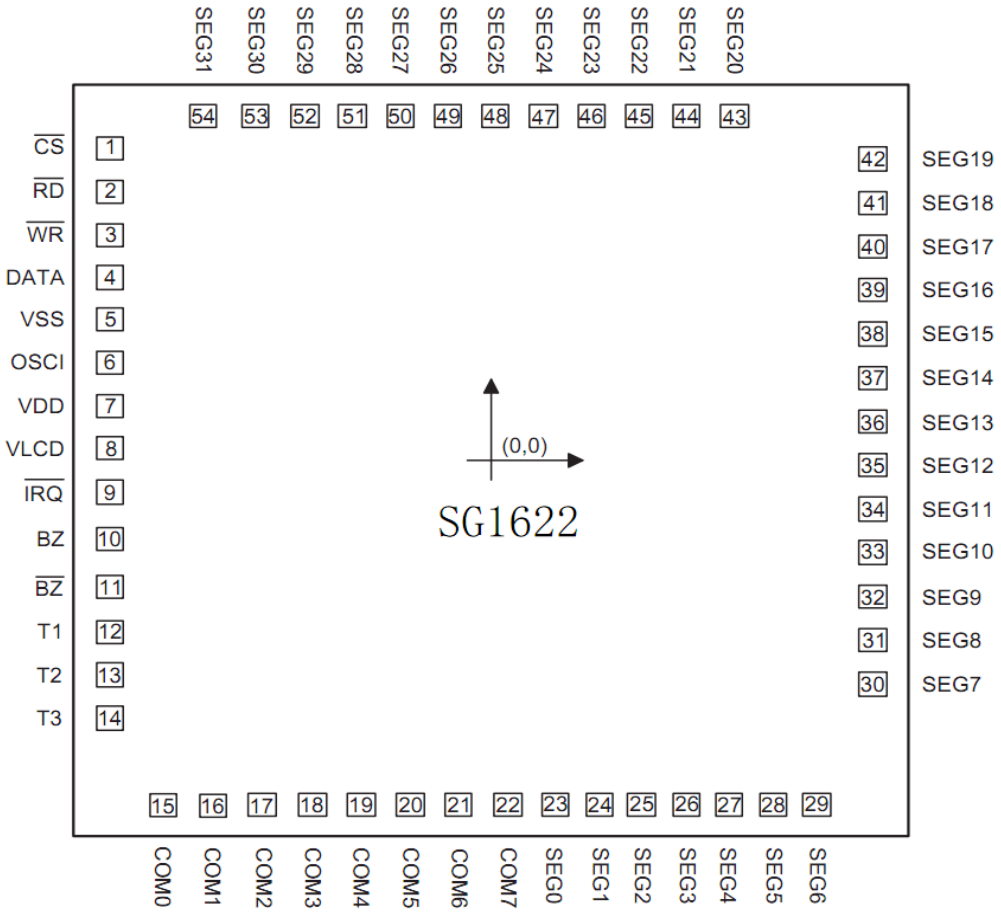
Block Diagram



Pad Assignment



IC衬底接VDD或悬空

芯片尺寸：1910*1910um²

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Pad Coordinates

NO	NAME	X	Y
1	CSB	-775.200	827.600
2	RDB	-775.200	717.600
3	WRB	-775.200	607.600
4	DATA	-775.200	497.600
5	VSS	-775.200	373.600
6	OSCI	-775.200	263.600
7	VDD	-775.200	153.600
8	VLCD	-775.200	-43.600
9	IRQB	-775.200	-66.400
10	BZ	-775.200	-176.400
11	BZB	-775.200	-303.600
12	T1	-775.200	-413.600
13	T2	-775.200	-523.600
14	T3	-775.200	-633.600
15	COM0	-728.900	-828.500
16	COM1	-618.900	-828.500
17	COM2	-508.900	-828.500
18	COM3	-398.900	-828.500
19	COM4	-288.900	-828.500
20	COM5	-178.900	-828.500
21	COM6	-68.900	-828.500
22	COM7	41.100	-828.500
23	SEG0	151.100	-828.500
24	SEG1	261.100	-828.500
25	SEG2	371.100	-828.500
26	SEG3	481.100	-828.500
27	SEG4	591.100	-828.500

NO	NAME	X	Y
28	SEG5	701.100	-828.500
29	SEG6	811.050	-828.450
30	SEG7	828.550	-562.850
31	SEG8	828.550	-452.850
32	SEG9	828.550	-342.850
33	SEG10	828.550	-232.850
34	SEG11	828.550	-122.850
35	SEG12	828.550	-12.850
36	SEG13	828.550	97.150
37	SEG14	828.550	207.150
38	SEG15	828.550	317.150
39	SEG16	828.550	427.150
40	SEG17	828.550	537.150
41	SEG18	828.550	647.150
42	SEG19	828.550	757.150
43	SEG20	670.950	828.500
44	SEG21	560.950	828.500
45	SEG22	450.950	828.500
46	SEG23	340.950	828.500
47	SEG24	230.950	828.500
48	SEG25	120.950	828.500
49	SEG26	10.950	828.500
50	SEG27	-99.050	828.500
51	SEG28	-209.050	828.500
52	SEG29	-319.050	828.500
53	SEG30	-429.050	828.500
54	SEG31	-539.050	828.500

Pad Description

Pad No.	Pad Name	I/O	Description
1	$\overline{CS}$	I	Chip selection input with Pull-high resistor. When the $\overline{CS}$ is logic high, the data and command read from or written to the SG1622 are disabled. The serial interface circuit is also reset. But if $\overline{CS}$ is at logic low level and is input to the $\overline{CS}$ pad, the data and command transmission between the host controller and the SG1622 are all enabled.
2	$\overline{RD}$	I	READ clock input with Pull-high resistor. Data in the RAM of the SG1622 are clocked out on the falling edge of the $\overline{RD}$ signal. The clocked out data will appear on the data line. The host controller can use the next rising edge to latch the clocked out data.
3	$\overline{WR}$	I	WRITE clock input with Pull-high resistor. Data on the DATA line are latched into the SG1622 on the rising edge of the $\overline{WR}$ signal.
4	DATA	I/O	Serial data input or output with Pull-high resistor
5	VSS	—	Negative power supply, ground
6	OSCI	I	If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad.
7	VDD	—	Positive power supply
8	VLCD	I	LCD operating voltage input pad
9	$\overline{IRQ}$	O	Time base or Watchdog Timer overflow flag, NMOS open drain output
10, 11	BZ, $\overline{BZ}$	O	2kHz or 4kHz tone frequency output pair
12~14	T1~T3	I	Not connected
15~22	COM0~COM7	O	LCD common outputs
23~54	SEG0~SEG31	O	LCD segment outputs

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Absolutely max. ratings

Characteristics	Symbol	Rating	Unit
Supply Voltage	Vdd	5.5	V
Input Voltage	Vin	Vss-0.3 to Vdd+0.3	V
Operating Temperature	Top	-25℃- +75℃	℃
Storage Temperature	Tsto	-50℃- +125℃	℃

D.C. Characteristics

Characteristics	Symbol	Test Condition and Vdd Voltage		Min.	Typ.	Max.	unit
Operating voltage	VDD			2.7	3	5.5	V
Operating current 1	I_{OP1}	Built-in oscillator on, LCD on, No load	3V		80	210	uA
			5V		135	415	
Operating current 2	I_{OP2}	Built-in oscillator on, LCD off, No load	3V		8	30	uA
			5V		20	55	
Stand-by current	Istb	Oscillator off, System halt, LCD off, No load	3V		1	8	uA
			5V		2	16	
Input Low Voltage	V_{IL1}	at RD/ WR/ DATA/CS	3V	0		0.6	V
			5V	0		1.0	
Input High Voltage	V_{IH1}	at RD/ WR/ DATA/CS	3V	2.4		3	V
			5V	4.0		5.0	
Output Source Current	I_{OH1}	VOH=2.7 at DATA	3V	-200	-450		uA
		VOH=4.5 at DATA	5V	-250	-500		
Output Sink Current	I_{OL1}	VOL=0.3V at DATA	3V	200	450		uA
		VOL=0.5V at DATA	5V	250	500		
Segment output 'H' Current	IS_{OH}	VOH=2.7 at SEG0-SEG31	3V	-6	-13		uA
		VOH=4.5 at SEG0-SEG31	5V	-20	-40		
Segment output 'L' Current	IS_{OL}	VOL=0.3V at SEG0-SEG31	3V	15	30		uA
		VOL=0.5V at SEG0-SEG31	5V	70	150		
Common output 'H' Current	IC_{OH}	VOH=2.7 at COM0-COM7	3V	-15	-30		uA
		VOH=4.5 at COM0-COM7	5V	-45	-90		
Common output 'L' Current	IC_{OL}	VOL=0.3V at COM0-COM7	3V	15	40		uA
		VOL=0.5V at COM0-COM7	5V	100	200		
Pull-High Resistor	R_{PH}	at $\overline{RD}$/ WR/ DATA/CS	3V	100	200	300	kΩ
			5V	50	100	150	

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A.C. Characteristics

Characteristics	Symbol	Test Condition		Min.	Typ.	Max.	unit
System clock 1	f_{SYS1}	Built-in oscillator	3V	22	32	40	KHz
			5V	24	32	40	
System clock 2	f_{SYS2}	External clock			32		KHz
Interface Reset Pulse	T_{CS}	CS = 'L'			250		ns
Interface Write Pulse	T_{WR}	WR='L' at Vdd = 3.0V		3.34			us
Interface Read Pulse	T_{RD}	RD='L' at Vdd = 3.0V		6.67			us
Interface DATA Frequency	FD_{WR}	Write at Clock duty 50% at Vdd = 3.0V				150	KHz
	FD_{RD}	Read at Clock duty 50% at Vdd = 3.0V				75	KHz
LCD frame frequency	F_{LCD1}	32768Hz Crystal oscillator , LCD at 1/8 duty			64		HZ

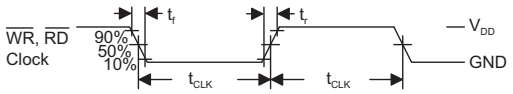

Figure 1

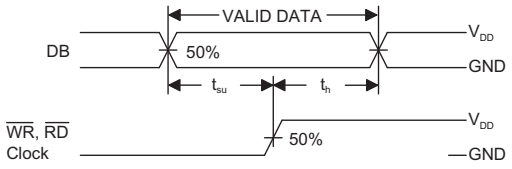

Figure 2

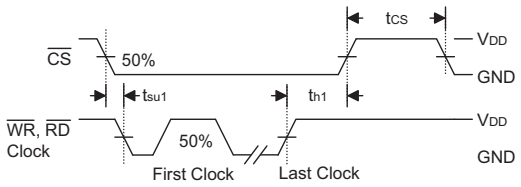

Figure 3

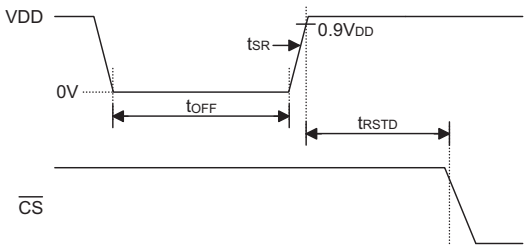

Figure 4. Power-on Reset Timing

Functional Description

Display Memory – RAM Structure

The static display RAM is organized into 64×4 bits and stores the display data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD patterns.

Time Base and Watchdog Timer (WDT)

The time base generator and WDT share the same divided (÷256) counter. TIMER DIS/EN/CLR, WDT DIS/EN/CLR and $\overline{IRQ}$ EN/DIS are independent from each other. Once the WDT time-out occurs, the $\overline{IRQ}$ pin will remain at logic low level until the CLR WDT or the $\overline{IRQ}$ DIS command is issued.

If an external clock is selected as the source of system frequency, the SYS DIS command turns out invalid and the power down mode fails to be carried out until the external clock source is removed.

Buzzer Tone Output

A simple tone generator is implemented in the SG1622. The tone generator can output a pair of differential driving signals on the BZ and $\overline{BZ}$ which are used to generate a single tone.

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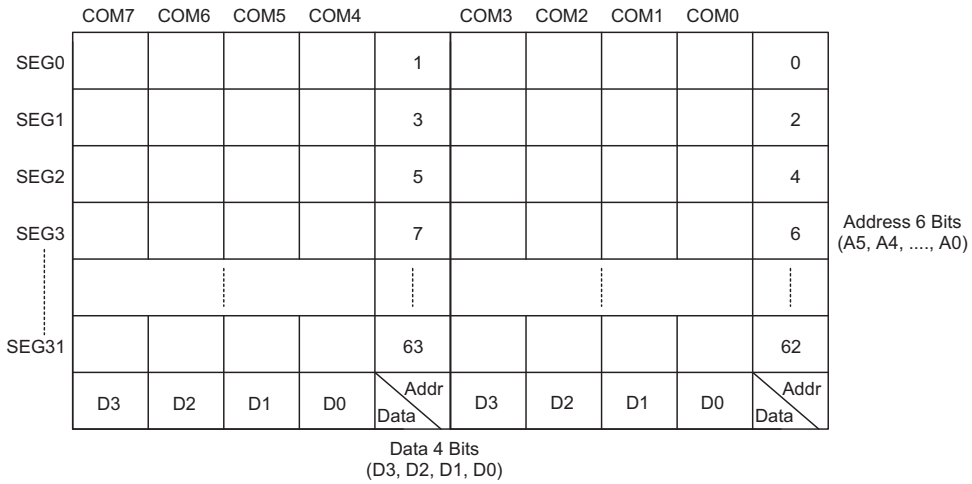
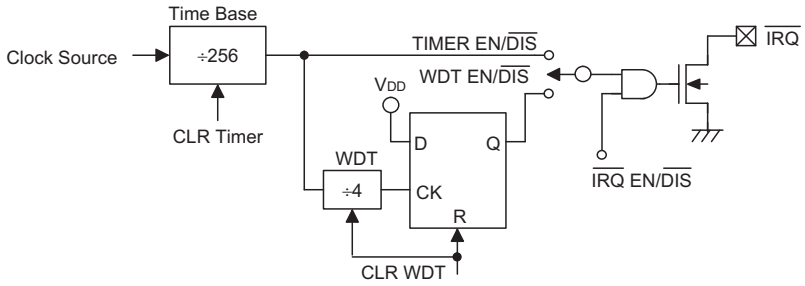


RAM Mapping



Timer and WDT Configurations

Command Format

The SG1622 can be configured by the software setting. There are two mode commands to configure the SG1622 resource and to transfer the LCD display data.

The following are the data mode ID and the command mode ID:

Operation	Mode	ID
READ	Data	1 1 0
WRITE	Data	1 0 1
READ-MODIFY-WRITE	Data	1 0 1
COMMAND	Command	1 0 0

If successive commands have been issued, the command mode ID can be omitted. While the system is operating in a non-successive command or a non-successive address data mode, the $\overline{CS}$ pin should be set to "1" and the previous operation mode will be reset also. The $\overline{CS}$ pin returns to "0", a new operation mode ID should be issued first.

Name	Command Code	Function
TONE OFF	0000-1000-X	Turn-off tone output
TONE 4K	010X-XXXX-X	Turn-on tone output, tone frequency is 4kHz
TONE 2K	0110-XXXX-X	Turn-on tone output, tone frequency is 2kHz

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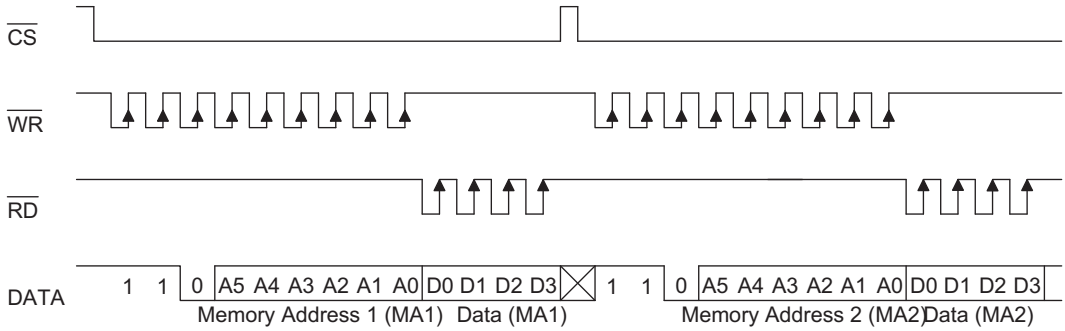
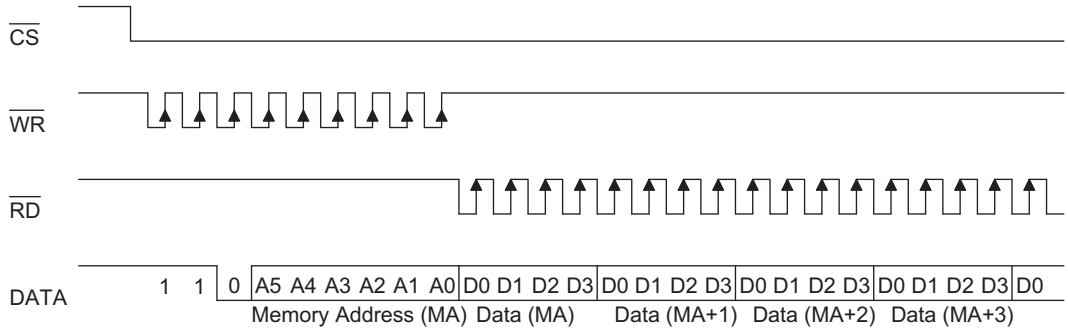
Timing Diagrams

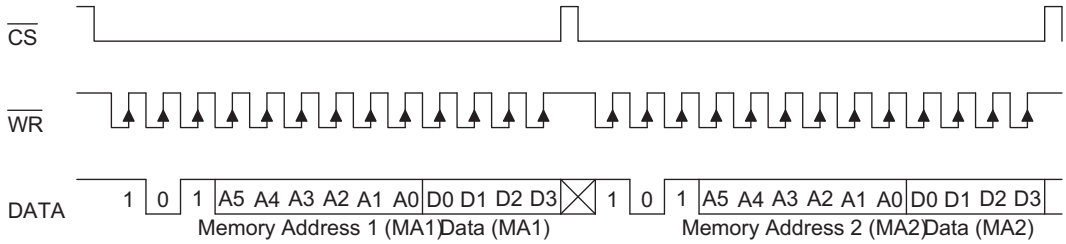
READ Mode (Command Code : 1 1 0)



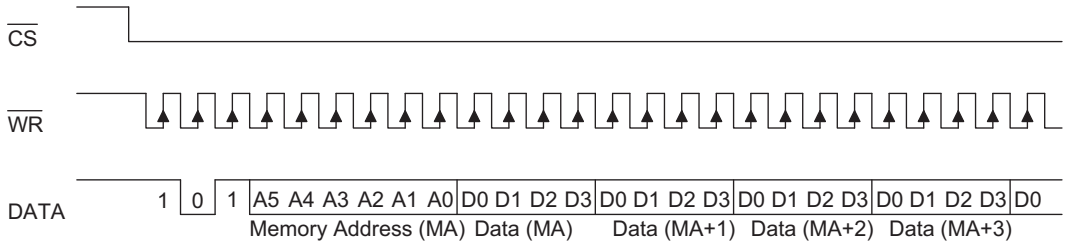
READ Mode (Successive Address Reading)



WRITE Mode (Command Code : 1 0 1)



WRITE Mode (Successive Address Writing)



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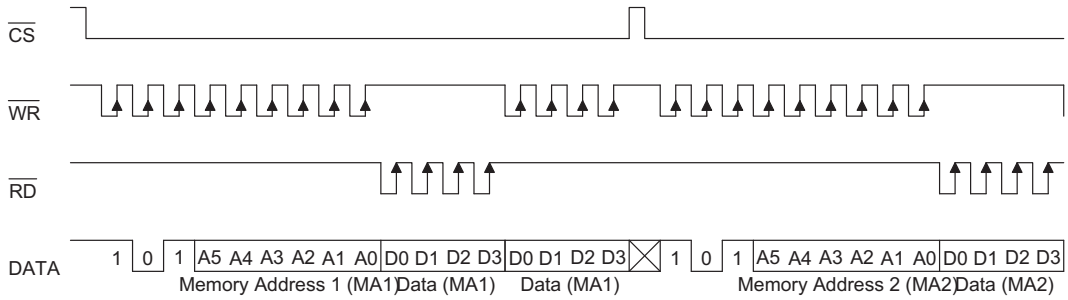
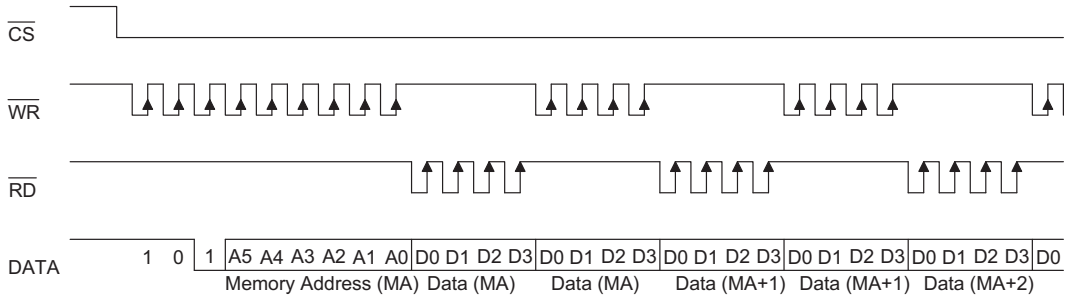
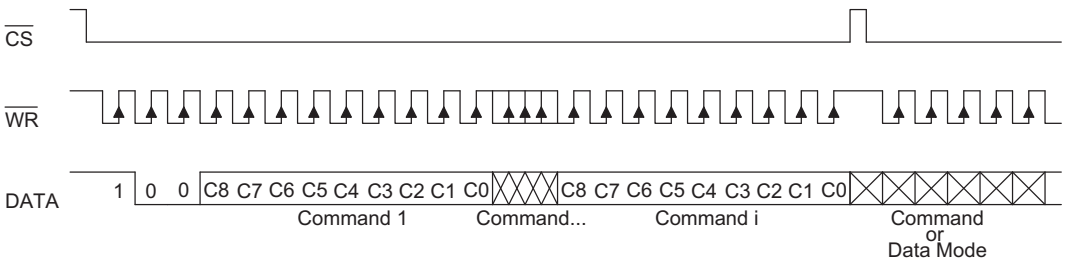
READ-MODIFY-WRITE Mode (Command Code : 1 0 1)



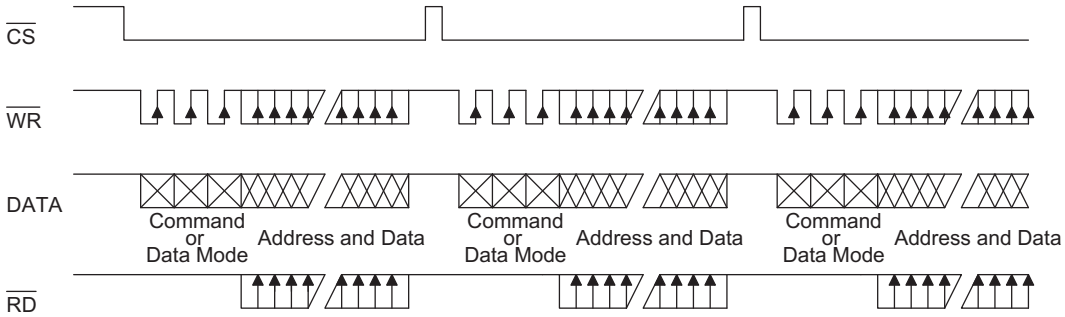
READ-MODIFY-WRITE Mode (Successive Address Accessing)



Command Mode (Command Code : 1 0 0)



Mode (Data and Command Mode)



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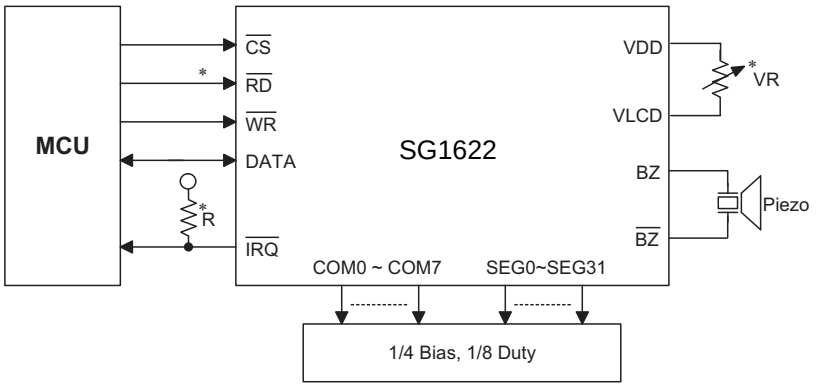
Application Circuits



LCD Panel

Note: The connection of $\overline{IRQ}$ and $\overline{RD}$ pin can be selected depending on the requirement of the MCU.
The voltage applied to V_{LCD} pin must be equal to or lower than V_{DD}.
Adjust VR to fit user's LCD panel display voltage (V_{LCD}).
Adjust R (external pull-high resistance) to fit user's time base clock.

Command Summary

Name	ID	Command Code	D/C	Function	Def.
READ	1 1 0	A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	1 0 1	A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	1 0 1	A5A4A3A2A1A0D0D1D2D3	D	Read and Write data to the RAM	
SYS DIS	1 0 0	0000-0000-X	C	Turn off both system oscillator and LCD bias generator	Yes
SYS EN	1 0 0	0000-0001-X	C	Turn on system oscillator	
LCD OFF	1 0 0	0000-0010-X	C	Turn off LCD display	Yes
LCD ON	1 0 0	0000-0011-X	C	Turn on LCD display	
TIMER DIS	1 0 0	0000-0100-X	C	Disable time base output	Yes
WDT DIS	1 0 0	0000-0101-X	C	Disable WDT time-out flag output	Yes
TIMER EN	1 0 0	0000-0110-X	C	Enable time base output	
WDT EN	1 0 0	0000-0111-X	C	Enable WDT time-out flag output	
TONE OFF	1 0 0	0000-1000-X	C	Turn off tone outputs	Yes
CLR TIMER	1 0 0	0000-1101-X	C	Clear the contents of the time base generator	
CLR WDT	1 0 0	0000-1111-X	C	Clear the contents of WDT stage	
RC 32K	1 0 0	0001-10XX-X	C	System clock source, on-chip RC oscillator	Yes
EXT 32K	1 0 0	0001-11XX-X	C	System clock source, external clock source	
TONE 4K	1 0 0	010X-XXXX-X	C	Tone frequency output: 4kHz	
TONE 2K	1 0 0	0110-XXXX-X	C	Tone frequency output: 2kHz	
$\overline{IRQ}$ DIS	1 0 0	100X-0XXX-X	C	Disable $\overline{IRQ}$ output	Yes
$\overline{IRQ}$ EN	1 0 0	100X-1XXX-X	C	Enable $\overline{IRQ}$ output	

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Name	ID	Command Code	D/C	Function	Def.
F1	**1 0 0**	101X-0000-X	C	Time base clock output: 1Hz The WDT time-out flag after: 4s	
F2	**1 0 0**	101X-0001-X	C	Time base clock output: 2Hz The WDT time-out flag after: 2s	
F4	**1 0 0**	101X-0010-X	C	Time base clock output: 4Hz The WDT time-out flag after: 1s	
F8	**1 0 0**	101X-0011-X	C	Time base clock output: 8Hz The WDT time-out flag after: 1/2s	
F16	**1 0 0**	101X-0100-X	C	Time base clock output: 16Hz The WDT time-out flag after: 1/4s	
F32	**1 0 0**	101X-0101-X	C	Time base clock output: 32Hz The WDT time-out flag after: 1/8s	
F64	**1 0 0**	101X-0110-X	C	Time base clock output: 64Hz The WDT time-out flag after: 1/16s	
F128	**1 0 0**	101X-0111-X	C	Time base clock output: 128Hz The WDT time-out flag after: 1/32s	Yes
TEST	**1 0 0**	1110-0000-X	C	Test mode, user don't use.	
NORMAL	**1 0 0**	1110-0011-X	C	Normal mode	Yes

Note: X : Don't care

A5~A0 : RAM address

D3~D0 : RAM data

D/C : Data/Command mode

Def. : Power on reset default

All the bold forms, namely **1 1 0**, **1 0 1**, and **1 0 0**, are mode commands. Of these, **1 0 0** indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The source of the tone frequency and of the time base or WDT clock frequency can be derived from an on-chip 32kHz RC oscillator or an external 32768Hz clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the SG1622 after power on reset, for power on reset may fail, which in turn leads to the malfunctioning of the SG1622.

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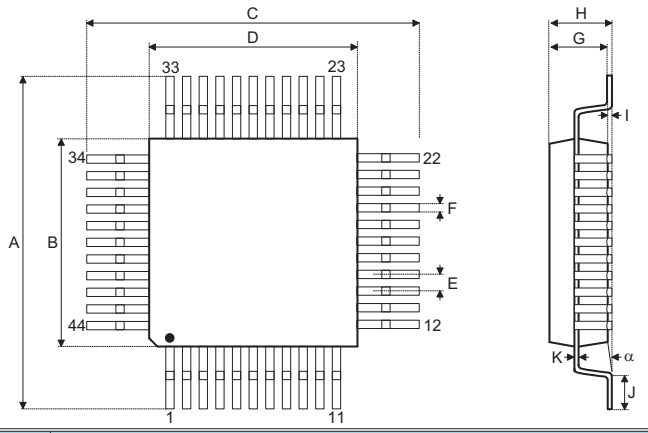
44-pin LQFP (10mm×10mm) (FP2.0mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.472 BSC	—
B	—	0.394 BSC	—
C	—	0.472 BSC	—
D	—	0.394 BSC	—
E	—	0.032 BSC	—
F	0.012	0.015	0.018
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	12.00 BSC	—
B	—	10.00 BSC	—
C	—	12.00 BSC	—
D	—	10.00 BSC	—
E	—	0.80 BSC	—
F	0.30	0.37	0.45
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

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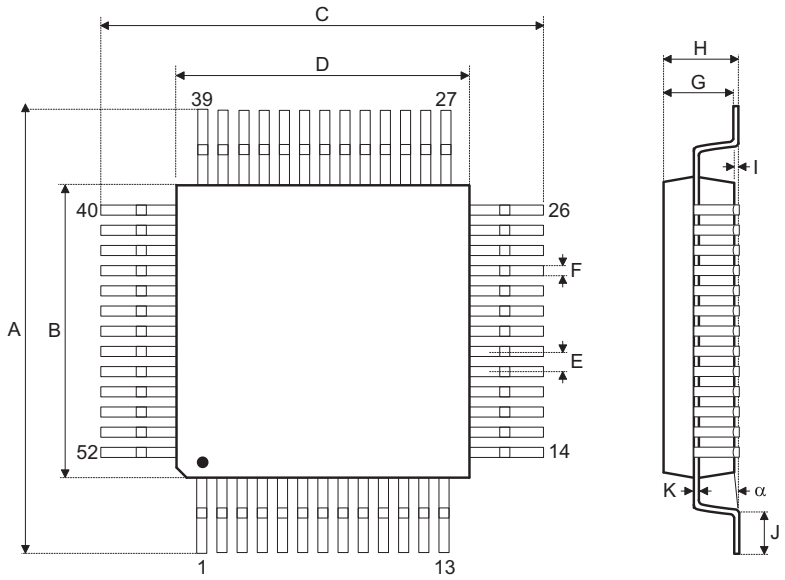
52-pin LQFP (14mm×14mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.622	0.630	0.638
B	0.547	0.551	0.555
C	0.622	0.630	0.638
D	0.547	0.551	0.555
E	—	0.039 BSC	—
F	0.015	—	0.019
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.008
J	0.018	—	0.030
K	0.005	—	0.007
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	15.80	16.00	16.20
B	13.90	14.00	14.10
C	15.80	16.00	16.20
D	13.90	14.00	14.10
E	—	1.0 BSC	—
F	0.39	—	0.48
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.20
J	0.45	—	0.75
K	0.13	—	0.18
α	0°	—	7°

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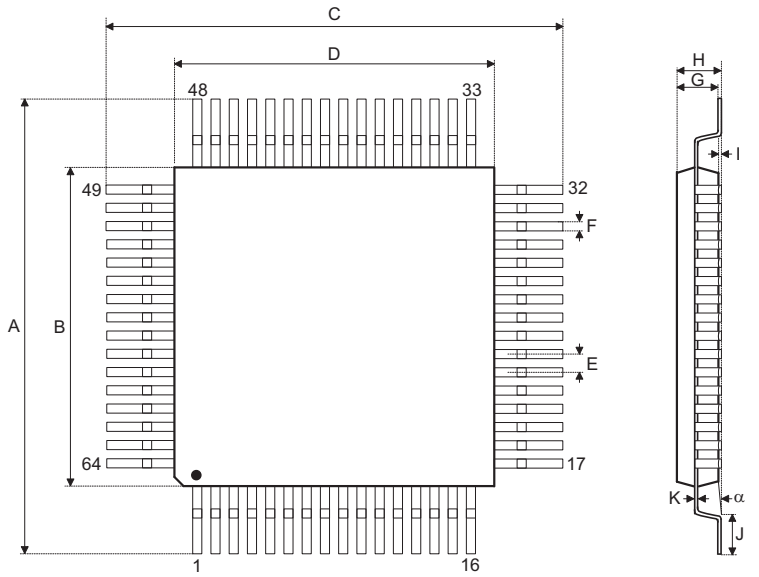
64-pin LQFP (7mm×7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.020 BSC	—
F	0.005	0.007	0.009
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.00 BSC	—
B	—	7.00 BSC	—
C	—	9.00 BSC	—
D	—	7.00 BSC	—
E	—	0.40 BSC	—
F	0.13	0.18	0.23
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

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